

FIG.1

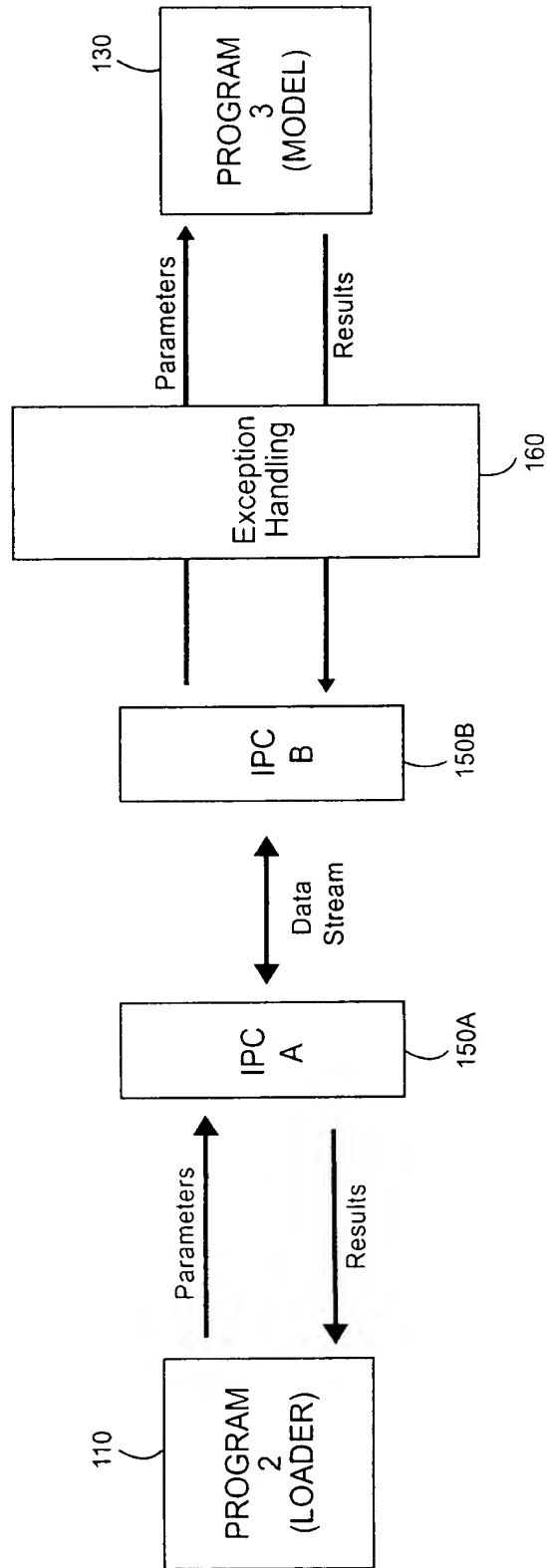


FIG. 2

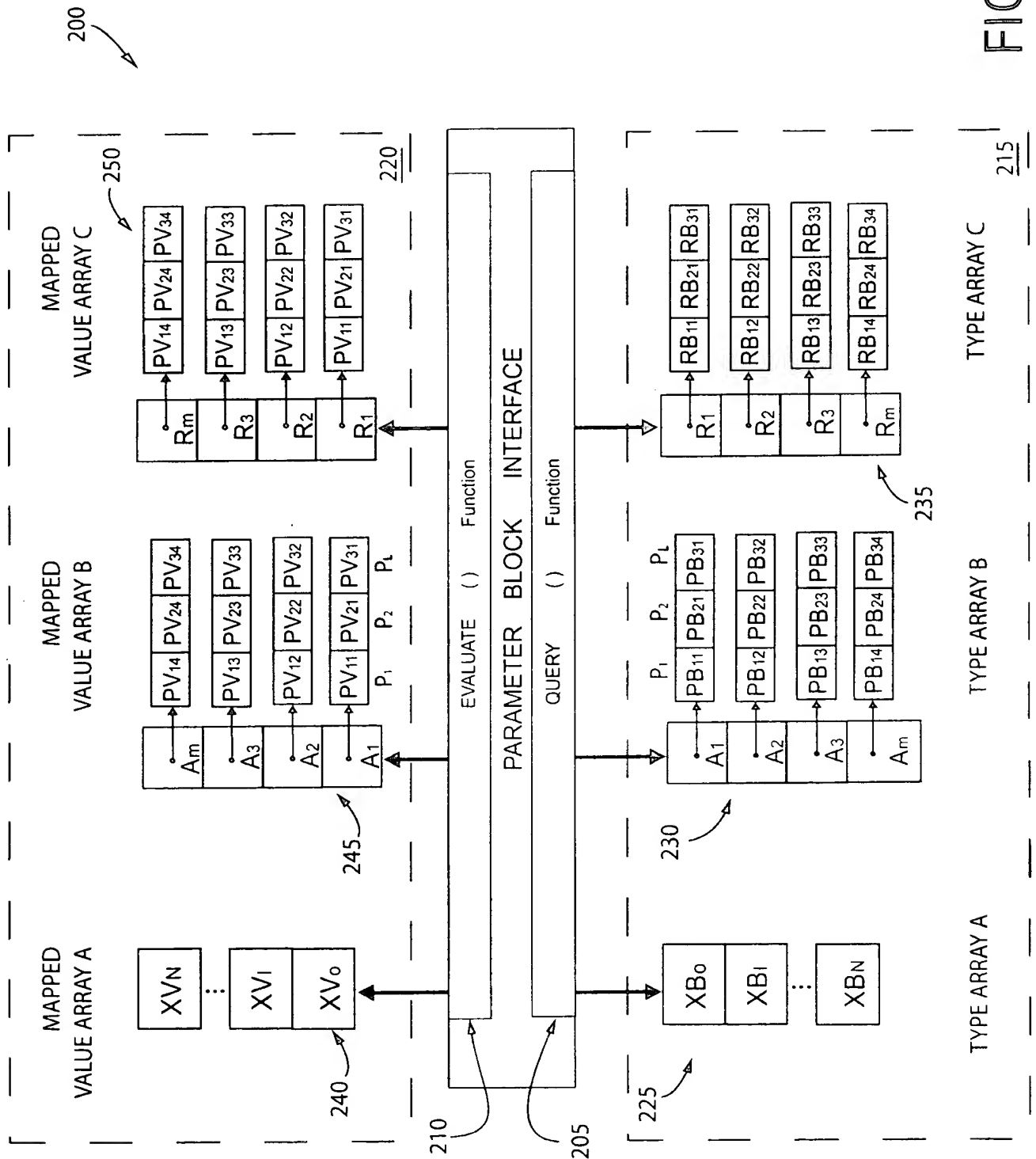


FIG.3

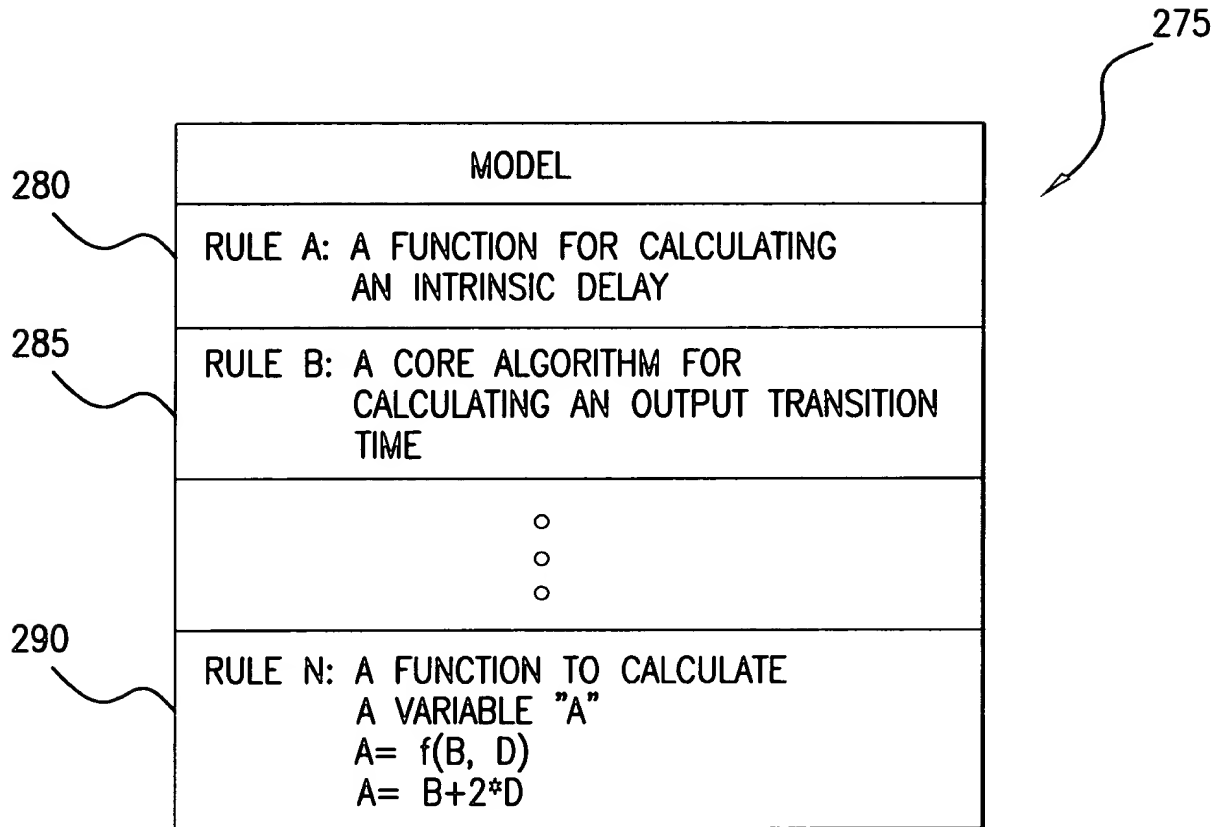


FIG. 4

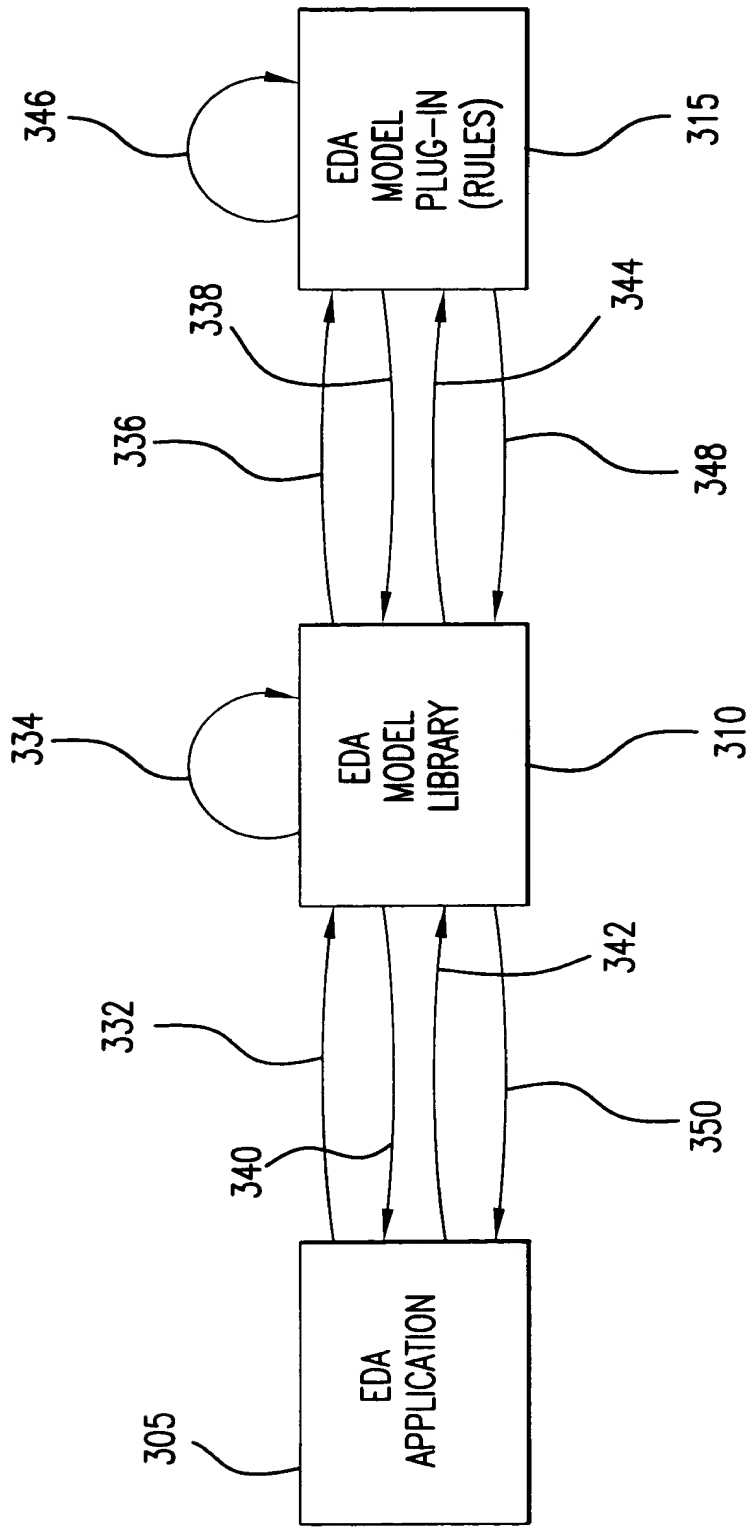


FIG. 5

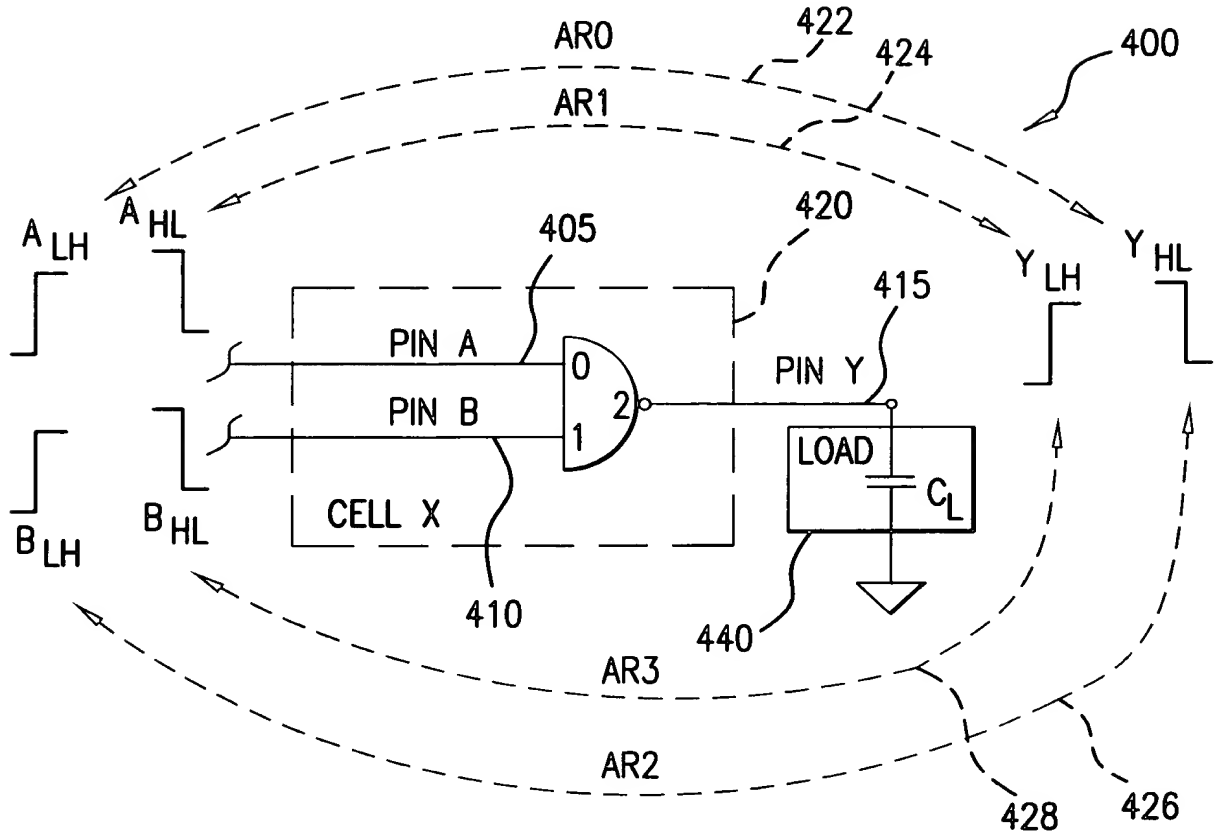


FIG. 6A

ARC RULES	INPUT AT		OUTPUT AT
	PIN A	PIN B	PIN Y
AR0	A _{LH}	I	Y _{HL}
AR1	A _{HL}	I	Y _{LH}
AR2	I	B _{LH}	Y _{HL}
AR3	I	B _{HL}	Y _{LH}

FIG. 6B

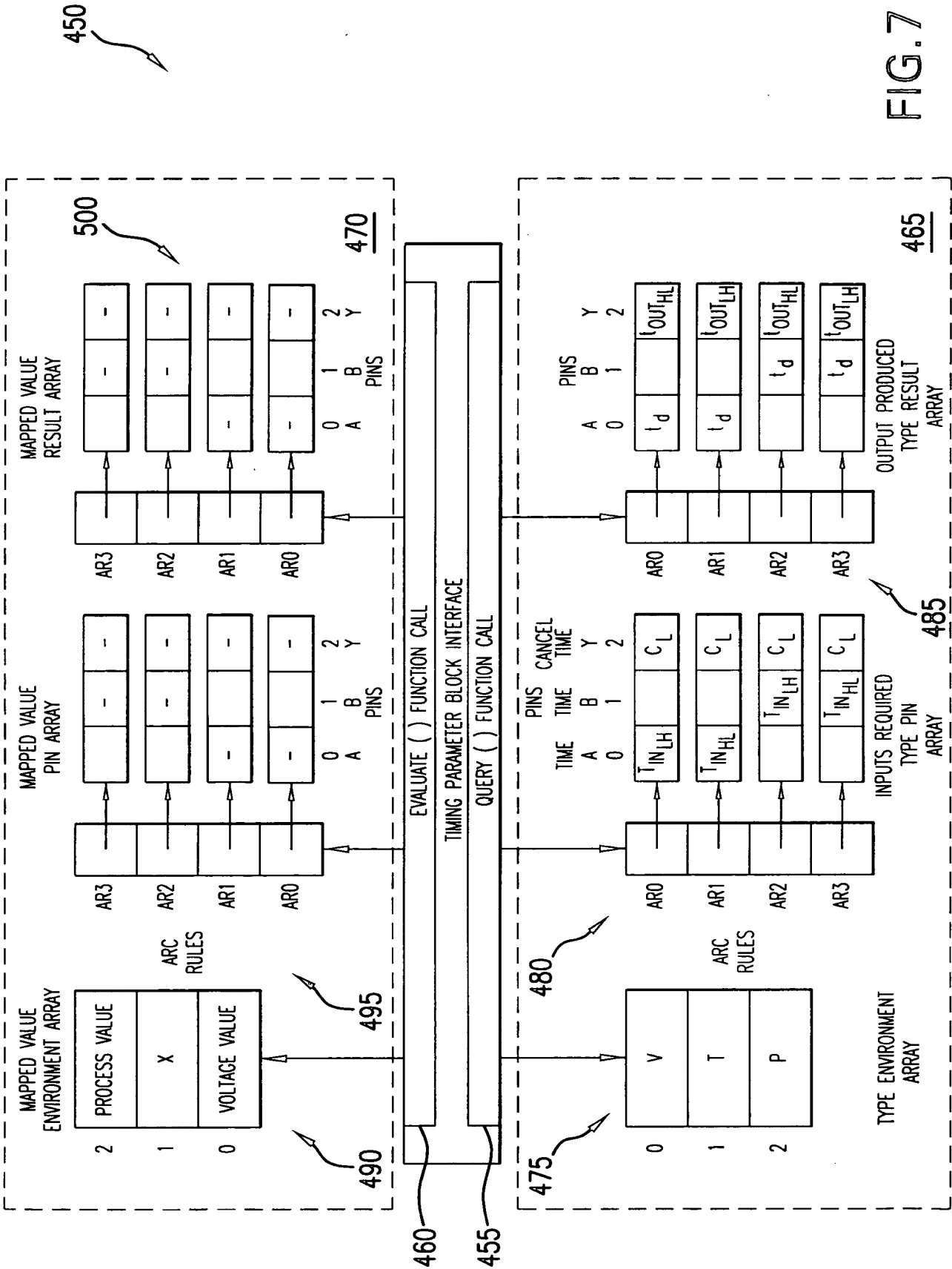


FIG. 7

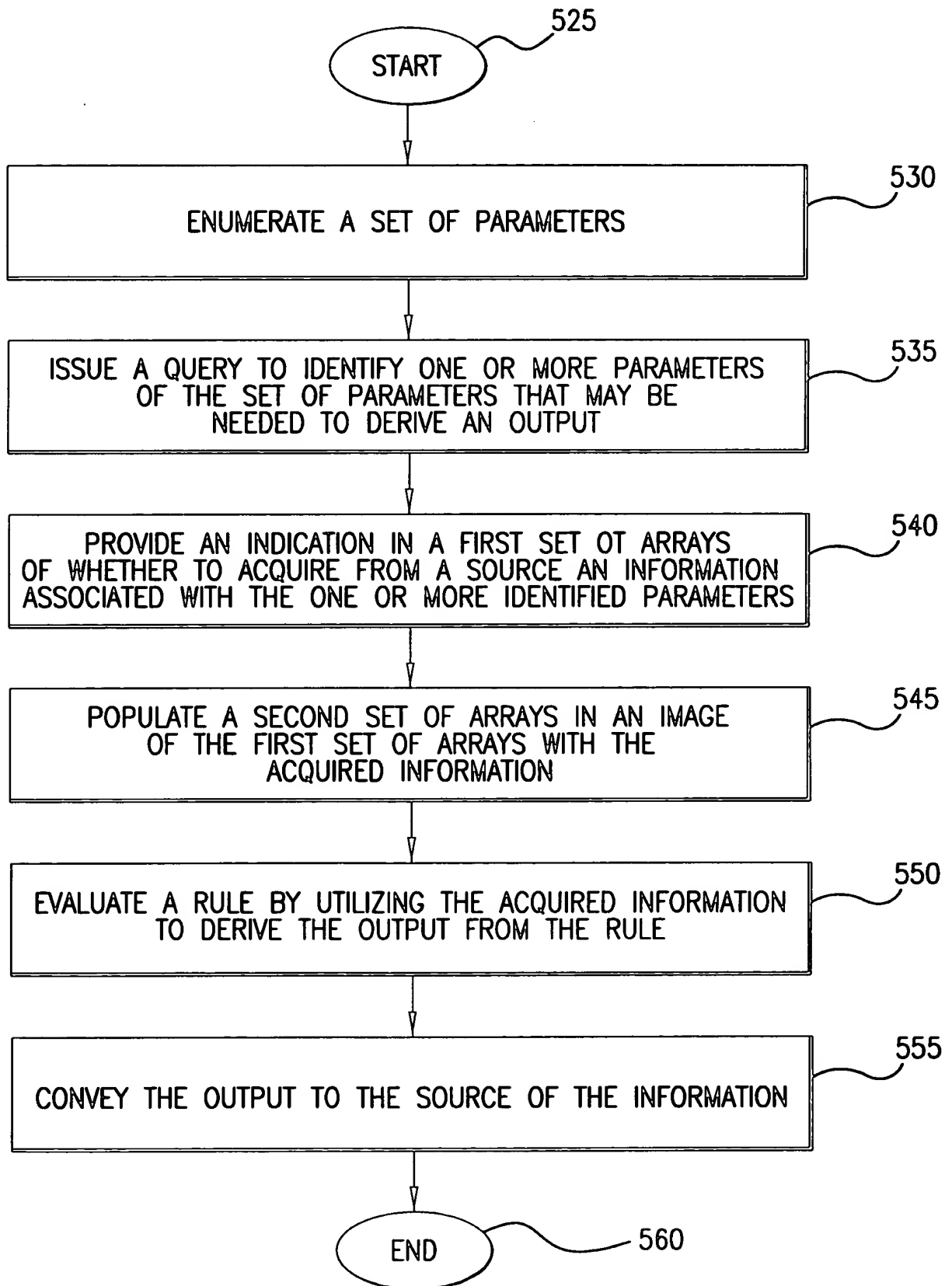


FIG.8A

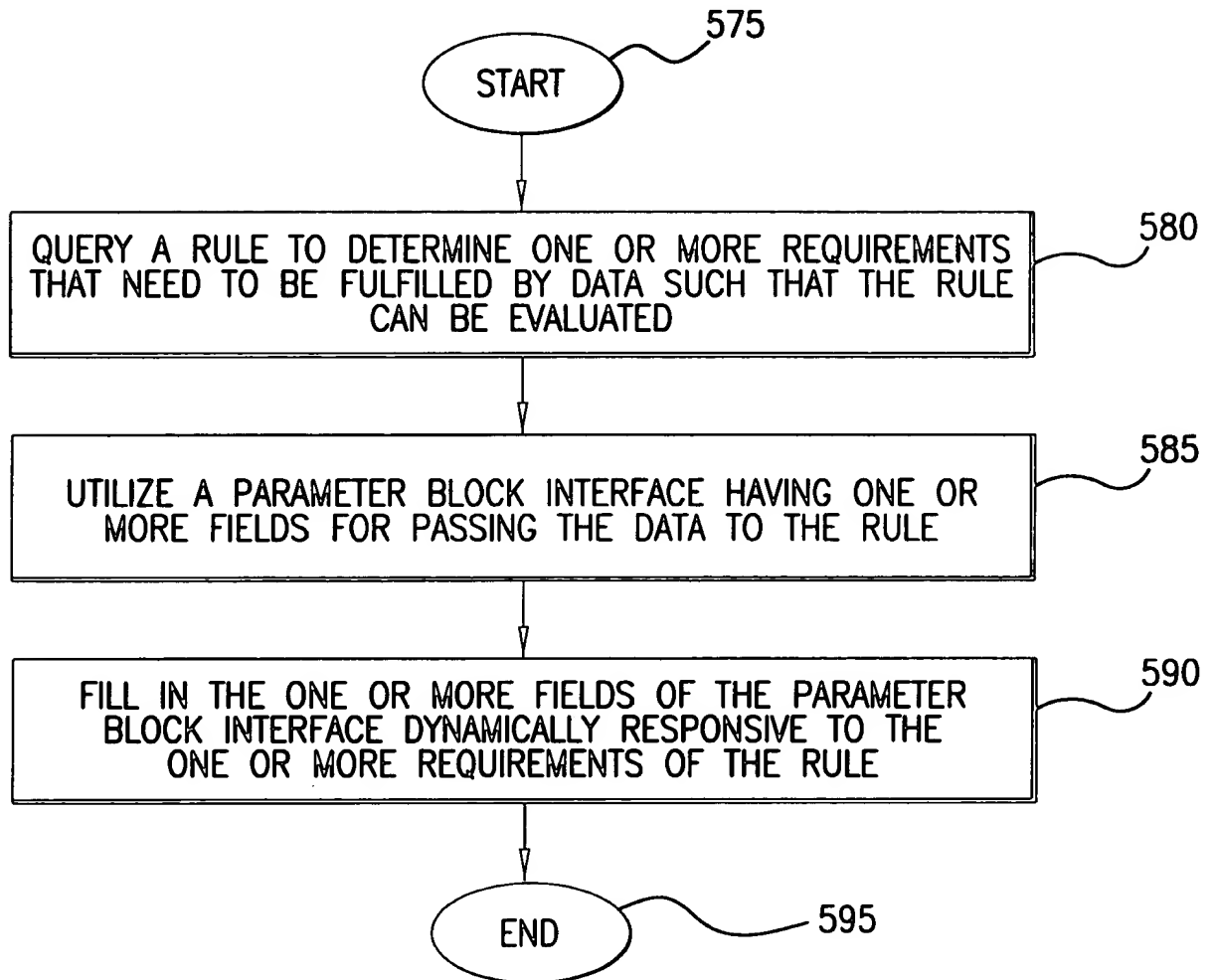


FIG. 8B